Beaglebone Black PRU Input P8/P9 Header PinMux Modes

PRU 0 Inputs	P8/P9 Pin	Offset	mode0	mode1	mode2	mode3	mode4	mode5	mode6	mode7	GPIO #
PRU0_R31_0	P9_31	0x990	mcasp0_aclkx	ehrpwm0A		spi1_sclk	mmc0_sdcd	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	gpio3_14	110
PRU0_R31_1	P9_29	0x994	mcasp0_fsx	ehrpwm0B		spi1_d0	mmc1_sdcd	pr1_pru0_pru_r30_1	pr1_pru0_pru_r31_1	gpio3_15	111
PRU0_R31_2	P9_30	0x998	mcasp0_axr0	ehrpwm0_tripzone_input		spi1_d1	mmc2_sdcd	pr1_pru0_pru_r30_2	pr1_pru0_pru_r31_2	gpio3_16	112
PRU0_R31_3	P9_28	0x99C	mcasp0_ahclkr	ehrpwm0_synci	mcasp0_axr2	spi1_cs0	eCAP2_in_PWM2_out	pr1_pru0_pru_r30_3	pr1_pru0_pru_r31_3	gpio3_17	113
PRU0_R31_4	P9_42.1	0x9A0	mcasp0_aclkr	eQEP0A_in	mcasp0_axr2	mcasp1_aclkx	mmc0_sdwp	pr1_pru0_pru_r30_4	pr1_pru0_pru_r31_4	gpio3_18	114
PRU0_R31_5	P9_27	0x9A4	mcasp0_fsr	eQEP0B_in	mcasp0_axr3	mcasp1_fsx	EMU2	pr1_pru0_pru_r30_5	pr1_pru0_pru_r31_5	gpio3_19	115
PRU0_R31_6	P9_41.1	0x9A8	mcasp0_axr1	eQEP0_index		mcasp1_axr0	EMU3	pr1_pru0_pru_r30_6	pr1_pru0_pru_r31_6	gpio3_20	116
PRU0_R31_7	P9_25	0x9AC	mcasp0_ahclkx	eQEP0_strobe	mcasp0_axr3	mcasp1_axr1	EMU4	pr1_pru0_pru_r30_7	pr1_pru0_pru_r31_7	gpio3_21	117
PRU0_R31_14	P8_16	0x838	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index	pr1_mii0_txd0	pr1_pru0_pru_r31_14	gpio1_14	46
PRU0_R31_15	P8_15	0x83C	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe	pr1_ecap0_ecap_capin_apwm_o	pr1_pru0_pru_r31_15	gpio1_15	47
PRU0_R31_16*	P9_24	0x984	uart1_txd	mmc2_sdwp	dcan1_rx	I2C1_SCL		pr1_uart0_txd	pr1_pru0_pru_r31_16	gpio0_15	15
PRU0_R31_16*	P9_41	0x9B4	xdma_event_intr1		tclkin	clkout2	timer7	pr1_pru0_pru_r31_16	EMU3	gpio0_20	20

PRU 1 Inputs	P8/P9 Pin	Offset	mode0	mode1	mode2	mode3	mode4	mode5	mode6	mode7	GPIO #
PRU1_R31_0	P8_45	0x8A0	lcd_data0	gpmc_a0	pr1_mii_mt0_clk	ehrpwm2A		pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	gpio2_6	70
PRU1_R31_1	P8_46	0x8A4	lcd_data1	gpmc_a1	pr1_mii0_txen	ehrpwm2B		pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	gpio2_7	71
PRU1_R31_2	P8_43	0x8A8	lcd_data2	gpmc_a2	pr1_mii0_txd3	ehrpwm2_tripzone_input		pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	gpio2_8	72
PRU1_R31_3	P8_44	0x8AC	lcd_data3	gpmc_a3	pr1_mii0_txd2	ehrpwm0_synco		pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	gpio2_9	73
PRU1_R31_4	P8_41	0x8B0	lcd_data4	gpmc_a4	pr1_mii0_txd1	eQEP2A_in		pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	gpio2_10	74
PRU1_R31_5	P8_42	0x8B4	lcd_data5	gpmc_a5	pr1_mii0_txd0	eQEP2B_in		pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	gpio2_11	75
PRU1_R31_6	P8_39	0x8B8	lcd_data6	gpmc_a6	pr1_edio_data_in6	eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	gpio2_12	76
PRU1_R31_7	P8_40	0x8BC	lcd_data7	gpmc_a7	pr1_edio_data_in7	eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	gpio2_13	77
PRU1_R31_8	P8_27	0x8E0	lcd_vsync	gpmc_a8	gpmc_a1	pr1_edio_data_in2	pr1_edio_data_out2	pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	gpio2_22	86
PRU1_R31_9	P8_29	0x8E4	lcd_hsync	gpmc_a9	gpmc_a2	pr1_edio_data_in3	pr1_edio_data_out3	pr1_pru1_pru_r30_9	pr1_pru1_pru_r31_9	gpio2_23	87
PRU1_R31_10	P8_28	0x8E8	lcd_pclk	gpmc_a10	pr1_mii0_crs	pr1_edio_data_in4	pr1_edio_data_out4	pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_10	gpio2_24	88
PRU1_R31_11	P8_30	0x8EC	lcd_ac_bias_en	gpmc_a11	pr1_mii1_crs	pr1_edio_data_in5	pr1_edio_data_out5	pr1_pru1_pru_r30_11	pr1_pru1_pru_r31_11	gpio2_25	89
PRU1_R31_12	P8_21	0x880	gpmc_csn1	gpmc_clk	mmc1_clk	pr1_edio_data_in6	pr1_edio_data_out6	pr1_pru1_pru_r30_12	pr1_pru1_pru_r31_12	gpio1_30	62
PRU1_R31_13	P8_20	0x884	gpmc_csn2	gpmc_be1n	mmc1_cmd	pr1_edio_data_in7	pr1_edio_data_out7	pr1_pru1_pru_r30_13	pr1_pru1_pru_r31_13	gpio1_31	63
PRU1_R31_16	P9_26	0x980	uart1_rxd	mmc1_sdwp	dcan1_tx	I2C1_SDA		pr1_uart0_rxd	pr1_pru1_pru_r31_16	gpio0_14	14

The information above shows the Pins on the Beaglebone Black P8 and P9 Headers which can be used in PRU0 or PRU1 as Inputs.

* Yes this is correct. Either P9_24 or P9_41 can be used as an input for PRU0 R31.t16

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Adapted from the open source pinmux.pdf document.

OfItselfSo.com/BeagleNotes/UsingDeviceTreesToConfigurePRUIOPins.php

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